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Class	Subclass
ISSUE CLASSIFICATION	

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED ~~IR~~ NS2 Q.A.	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/765958	D	~~702~~ 714	729	~~2857~~ 2123	Dooley

2133

APPLICANTS
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TITLE
Hierarchical test circuit structure for chips with multiple circuit blocks

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)						
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
INTERNATIONAL CLASSIFICATION								

☐ Continued on Issue Slip Inside File Jacket

☒ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to ________ (date) has been disclaimed.	(Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
☒ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. 6,631,504	(Primary Examiner) (Date)			ISSUE FEE	
				Amount Due	Date Paid
☐ The terminal ____ months of this patent have been disclaimed.	(Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER	

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